NEC

MOS INTEGRATED CIRCUIT

# μPD4481162, 4481182, 4481322, 4481362

## 8M-BIT ZEROSB™ SRAM PIPELINED OPERATION

### Description

The μPD4481162 is a 524,288-word by 16-bit, the μPD4481182 is a 524,288-word by 18-bit, the μPD4481322 is a 262,144-word by 32-bit and the μPD4481362 is a 262,144-word by 36-bit ZEROSB static RAM fabricated with advanced CMOS technology using full CMOS six-transistor memory cell.

The μPD4481162, μPD4481182, μPD4481322 and μPD4481362 are optimized to eliminate dead cycles for read to write, or write to read transitions. These ZEROSB static RAMs integrate unique synchronous peripheral circuitry, 2-bit burst counter and output buffer as well as SRAM core. All input registers are controlled by a positive edge of the single clock input (CLK).

The μPD4481162, μPD4481182, μPD4481322 and μPD4481362 are suitable for applications which require synchronous operation, high speed, low voltage, high density and wide bit configuration, such as buffer memory.

ZZ has to be set LOW at the normal operation. When ZZ is set HIGH, the SRAM enters Power Down State (“Sleep”). In the “Sleep” state, the SRAM internal state is preserved. When ZZ is set LOW again, the SRAM resumes normal operation.

The μPD4481162, μPD4481182, μPD4481322 and μPD4481362 are packaged in 100-pin PLASTIC LQFP with a 1.4 mm package thickness for high density and low capacitive loading.

### Features

★ • Low voltage core supply : $V_{DD}$ = 3.3 ± 0.165 V (-A44, -A50, -A60, -A75, -A44Y, -A50Y, -A60Y, -A75Y)
$V_{DD}$ = 2.5 ± 0.125 V (-C60, -C75, -C60Y, -C75Y)

- Synchronous operation

★ • Operating temperature : $T_A$ = 0 to 70 °C (-A44, -A50, -A60, -A75, -C60, -C75)
$T_A$ = –40 to +85 °C (-A44Y, -A50Y, -A60Y, -A75Y, -C60Y, -C75Y)

- 100 percent bus utilization
- Internally self-timed write control
- Burst read / write : Interleaved burst and linear burst sequence
- Fully registered inputs and outputs for pipelined operation
- All registers triggered off positive clock edge
- 3.3V or 2.5V LVTTL Compatible : All inputs and outputs
- Fast clock access time : 2.8 ns (225 MHz), 3.2 ns (200 MHz), 3.5 ns (167 MHz) , 4.2 ns (133 MHz)
- Asynchronous output enable : /G
- Burst sequence selectable : MODE
- Sleep mode : ZZ (ZZ = Open or Low : Normal operation)
- Separate byte write enable : /BW1 to /BW4 (μPD4481322 and μPD4481362)
/BW1 and /BW2 (μPD4481162 and μPD4481182)
- Three chip enables for easy depth expansion
- Common I/O using three state outputs



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**The mark ★ shows major revised points.**

★ **Ordering Information** (1/2)

| Part number | Access Time ns | Clock Frequency MHz | Core Supply Voltage V | I/O Interface | Operating Temperature °C | Package |
|---|---|---|---|---|---|---|
| μPD4481162GF-A44 | 2.8 | 225 | 3.3 ± 0.165 | 3.3 V LVTTL Note | 0 to 70 | 100-pin PLASTIC LQFP (14 x 20) |
| μPD4481162GF-A50 | 3.2 | 200 | | | | |
| μPD4481162GF-A60 | 3.5 | 167 | | 3.3 V or 2.5 V LVTTL | | |
| μPD4481162GF-A75 | 4.2 | 133 | | | | |
| μPD4481182GF-A44 | 2.8 | 225 | | 3.3 V LVTTL Note | | |
| μPD4481182GF-A50 | 3.2 | 200 | | | | |
| μPD4481182GF-A60 | 3.5 | 167 | | 3.3 V or 2.5 V LVTTL | | |
| μPD4481182GF-A75 | 4.2 | 133 | | | | |
| μPD4481322GF-A44 | 2.8 | 225 | | 3.3 V LVTTL Note | | |
| μPD4481322GF-A50 | 3.2 | 200 | | | | |
| μPD4481322GF-A60 | 3.5 | 167 | | 3.3 V or 2.5 V LVTTL | | |
| μPD4481322GF-A75 | 4.2 | 133 | | | | |
| μPD4481362GF-A44 | 2.8 | 225 | | 3.3 V LVTTL Note | | |
| μPD4481362GF-A50 | 3.2 | 200 | | | | |
| μPD4481362GF-A60 | 3.5 | 167 | | 3.3 V or 2.5 V LVTTL | | |
| μPD4481362GF-A75 | 4.2 | 133 | | | | |
| μPD4481162GF-C60 | 3.5 | 167 | 2.5 ± 0.125 | 2.5 V LVTTL | | |
| μPD4481162GF-C75 | 4.2 | 133 | | | | |
| μPD4481182GF-C60 | 3.5 | 167 | | | | |
| μPD4481182GF-C75 | 4.2 | 133 | | | | |
| μPD4481322GF-C60 | 3.5 | 167 | | | | |
| μPD4481322GF-C75 | 4.2 | 133 | | | | |
| μPD4481362GF-C60 | 3.5 | 167 | | | | |
| μPD4481362GF-C75 | 4.2 | 133 | | | | |

**Note** Although 2.5V LVTTL interface can also be used, a performance becomes equivalent to -A60 (167 MHz).

(2/2)

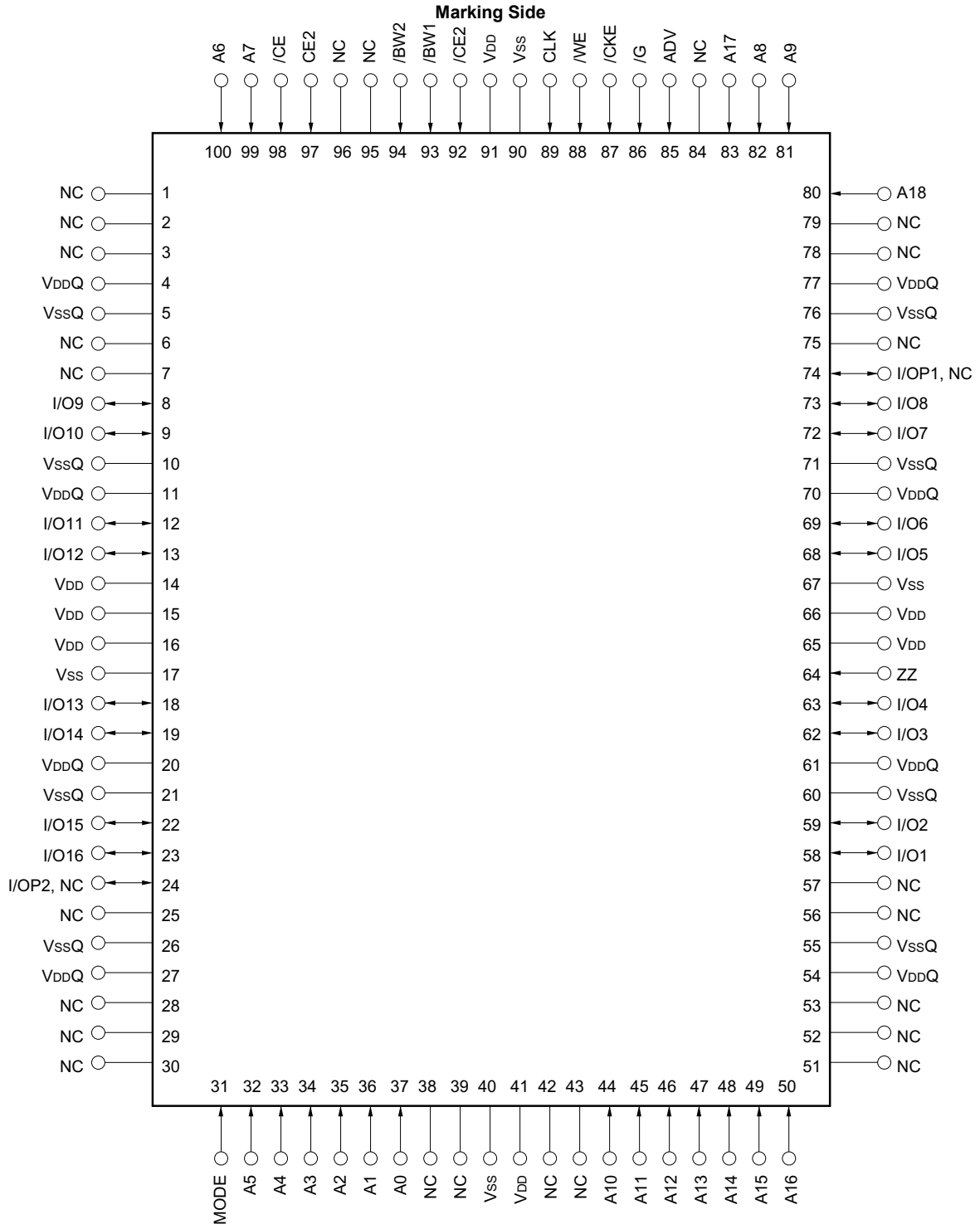
| Part number | Access Time ns | Clock Frequency MHz | Core Supply Voltage V | I/O Interface | Operating Temperature °C | Package |
|---|---|---|---|---|---|---|
| μPD4481162GF-A44Y | 2.8 | 225 | 3.3 ± 0.165 | 3.3 V LVTTL Note | −40 to +85 | 100-pin PLASTIC LQFP (14 x 20) |
| μPD4481162GF-A50Y | 3.2 | 200 | | | | |
| μPD4481162GF-A60Y | 3.5 | 167 | | 3.3 V or 2.5 V LVTTL | | |
| μPD4481162GF-A75Y | 4.2 | 133 | | | | |
| μPD4481182GF-A44Y | 2.8 | 225 | | 3.3 V LVTTL Note | | |
| μPD4481182GF-A50Y | 3.2 | 200 | | | | |
| μPD4481182GF-A60Y | 3.5 | 167 | | 3.3 V or 2.5 V LVTTL | | |
| μPD4481182GF-A75Y | 4.2 | 133 | | | | |
| μPD4481322GF-A44Y | 2.8 | 225 | | 3.3 V LVTTL Note | | |
| μPD4481322GF-A50Y | 3.2 | 200 | | | | |
| μPD4481322GF-A60Y | 3.5 | 167 | | 3.3 V or 2.5 V LVTTL | | |
| μPD4481322GF-A75Y | 4.2 | 133 | | | | |
| μPD4481362GF-A44Y | 2.8 | 225 | | 3.3 V LVTTL Note | | |
| μPD4481362GF-A50Y | 3.2 | 200 | | | | |
| μPD4481362GF-A60Y | 3.5 | 167 | | 3.3 V or 2.5 V LVTTL | | |
| μPD4481362GF-A75Y | 4.2 | 133 | | | | |
| μPD4481162GF-C60Y | 3.5 | 167 | 2.5 ± 0.125 | 2.5 V LVTTL | | |
| μPD4481162GF-C75Y | 4.2 | 133 | | | | |
| μPD4481182GF-C60Y | 3.5 | 167 | | | | |
| μPD4481182GF-C75Y | 4.2 | 133 | | | | |
| μPD4481322GF-C60Y | 3.5 | 167 | | | | |
| μPD4481322GF-C75Y | 4.2 | 133 | | | | |
| μPD4481362GF-C60Y | 3.5 | 167 | | | | |
| μPD4481362GF-C75Y | 4.2 | 133 | | | | |

**Note** Although 2.5V LVTTL interface can also be used, a performance becomes equivalent to -A60Y (167 MHz).

## Pin Configurations

/xxx indicates active low signal.

**100-pin PLASTIC LQFP (14 × 20)**
**[μPD4481162GF, μPD4481182GF]**




**Remark** Refer to **Package Drawing** for the 1-pin index mark.

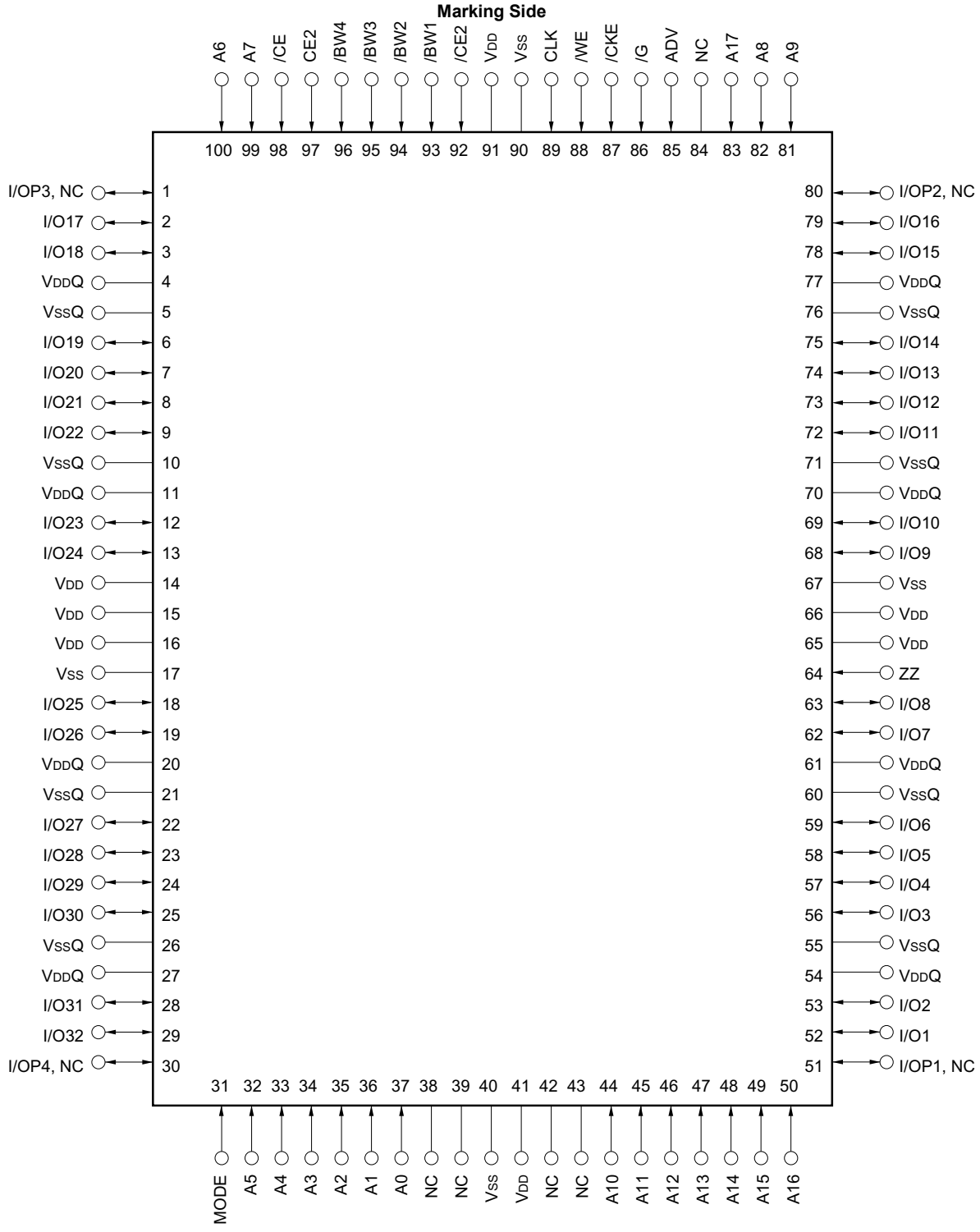
**Pin Identifications**

**[μPD4481162GF, μPD4481182GF]**

| Symbol | Pin No. | Description |
|---|---|---|
| A0 to A18 | 37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48, 49, 50, 83, 80 | Synchronous Address Input |
| I/O1 to I/O16 | 58, 59, 62, 63, 68, 69, 72, 73, 8, 9, 12, 13, 18, 19, 22, 23 | Synchronous Data In, Synchronous / Asynchronous Data Out |
| I/OP1, NC Note | 74 | Synchronous Data In (Parity), Synchronous / Asynchronous Data Out (Parity) |
| I/OP2, NC Note | 24 | |
| ADV | 85 | Synchronous Address Load / Advance Input |
| /CE, CE2, /CE2 | 98, 97, 92 | Synchronous Chip Enable Input |
| /WE | 88 | Synchronous Write Enable Input |
| /BW1, /BW2 | 93, 94 | Synchronous Byte Write Enable Input |
| /G | 86 | Asynchronous Output Enable Input |
| CLK | 89 | Clock Input |
| /CKE | 87 | Synchronous Clock Enable Input |
| MODE | 31 | Asynchronous Burst Sequence Select Input<br>Have to tied to $V_{DD}$ or $V_{SS}$ during normal operation |
| ZZ | 64 | Asynchronous Power Down State Input |
| $V_{DD}$ | 14, 15, 16, 41, 65, 66, 91 | Power Supply |
| $V_{SS}$ | 17, 40, 67, 90 | Ground |
| $V_{DD}Q$ | 4, 11, 20, 27, 54, 61, 70, 77 | Output Buffer Power Supply |
| $V_{SS}Q$ | 5, 10, 21, 26, 55, 60, 71, 76 | Output Buffer Ground |
| NC | 1, 2, 3, 6, 7, 25, 28, 29, 30, 38, 39, 42, 43, 51, 52, 53, 56, 57, 75, 78, 79, 84, 95, 96 | No Connection |

**Note** NC (No Connection) is used in the μPD4481162GF.
I/OP1 and I/OP2 are used in the μPD4481182GF.

**100-pin PLASTIC LQFP (14 × 20)**
**[μPD4481322GF, μPD4481362GF]**




**Remark** Refer to **Package Drawing** for the 1-pin index mark.

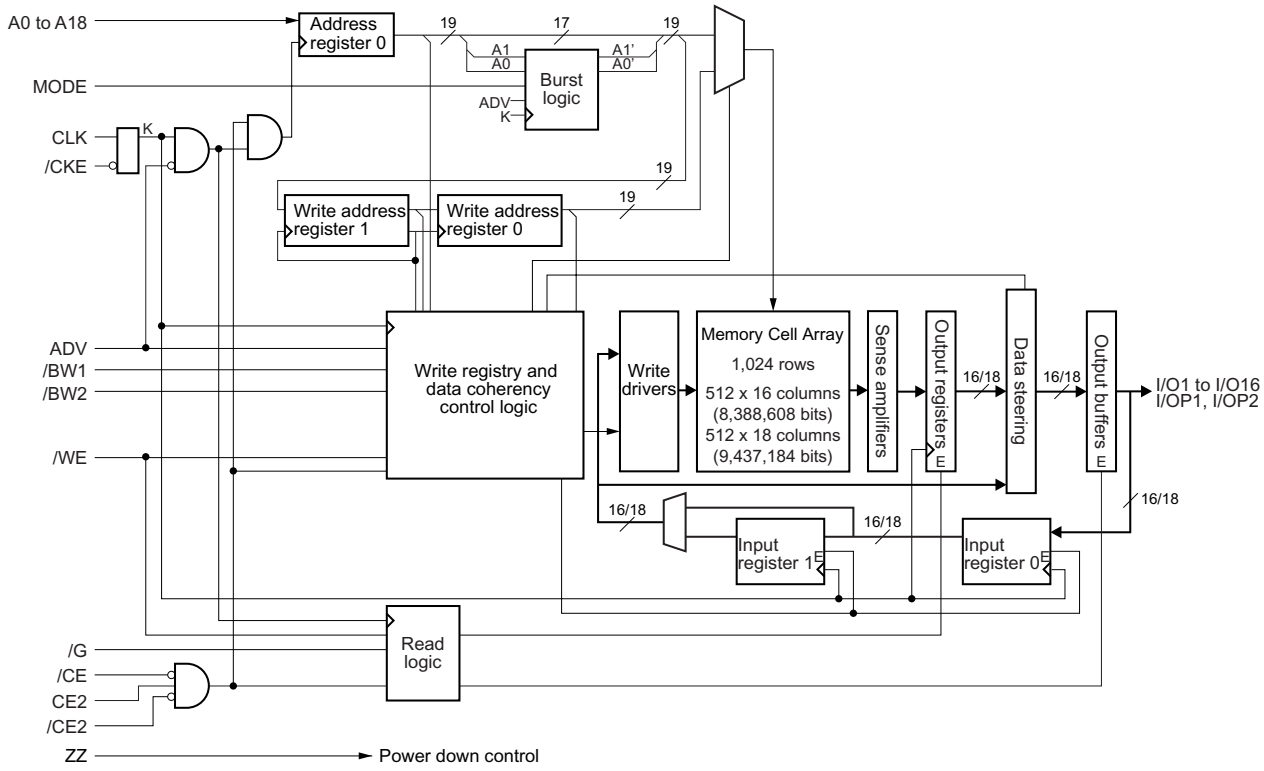
**[μPD4481322GF, μPD4481362GF]**

| Symbol | Pin No. | Description |
|---|---|---|
| A0 to A17 | 37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48, 49, 50, 83 | Synchronous Address Input |
| I/O1 to I/O32 | 52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 72, 73, 74, 75, 78, 79, 2, 3, 6, 7, 8, 9, 12, 13, 18, 19, 22, 23, 24, 25, 28, 29 | Synchronous Data In,<br>Synchronous / Asynchronous Data Out |
| I/OP1, NC Note | 51 | Synchronous Data In (Parity),<br>Synchronous / Asynchronous Data Out (Parity) |
| I/OP2, NC Note | 80 | |
| I/OP3, NC Note | 1 | |
| I/OP4, NC Note | 30 | |
| ADV | 85 | Synchronous Address Load / Advance Input |
| /CE, CE2, /CE2 | 98, 97, 92 | Synchronous Chip Enable Input |
| /WE | 88 | Synchronous Write Enable Input |
| /BW1 to /BW4 | 93, 94, 95, 96 | Synchronous Byte Write Enable Input |
| /G | 86 | Asynchronous Output Enable Input |
| CLK | 89 | Clock Input |
| /CKE | 87 | Synchronous Clock Enable Input |
| MODE | 31 | Asynchronous Burst Sequence Select Input<br>Have to tied to $V_{DD}$ or $V_{SS}$ during normal operation |
| ZZ | 64 | Asynchronous Power Down State Input |
| $V_{DD}$ | 14, 15, 16, 41, 65, 66, 91 | Power Supply |
| $V_{SS}$ | 17, 40, 67, 90 | Ground |
| $V_{DD}Q$ | 4, 11, 20, 27, 54, 61, 70, 77 | Output Buffer Power Supply |
| $V_{SS}Q$ | 5, 10, 21, 26, 55, 60, 71, 76 | Output Buffer Ground |
| NC | 38, 39, 42, 43, 84 | No Connection |

**Note** NC (No Connection) is used in the μPD4481322GF.
I/OP1 to I/OP4 are used in the μPD4481362GF.

## Block Diagrams

**[μPD4481162, μPD4481182]**




### Burst Sequence

**[μPD4481162, μPD4481182]**

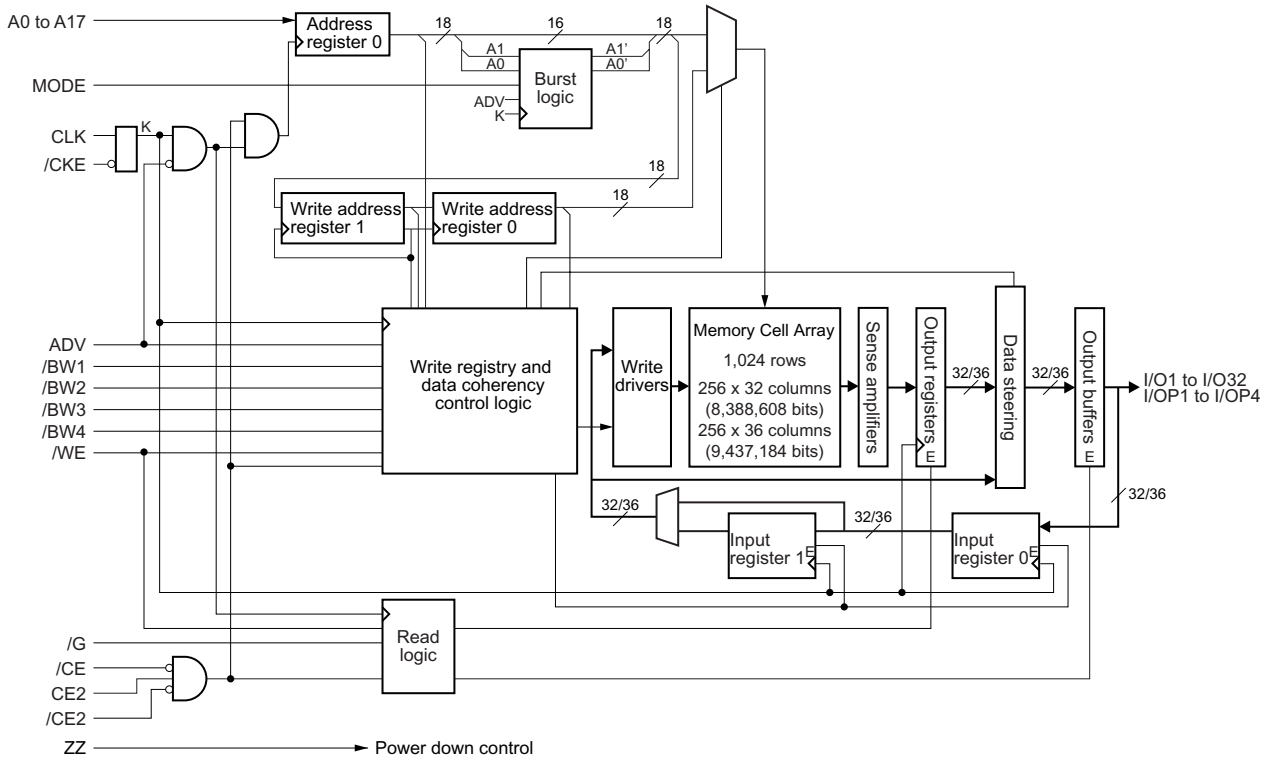
**Interleaved Burst Sequence Table (MODE = $V_{DD}$)**

| | |
|---|---|
| External Address | A18 to A2, A1, A0 |
| 1st Burst Address | A18 to A2, A1, /A0 |
| 2nd Burst Address | A18 to A2, /A1, A0 |
| 3rd Burst Address | A18 to A2, /A1, /A0 |

**Linear Burst Sequence Table (MODE = $V_{SS}$)**

| | | | | |
|---|---|---|---|---|
| External Address | A18 to A2, 0, 0 | A18 to A2, 0, 1 | A18 to A2, 1, 0 | A18 to A2, 1, 1 |
| 1st Burst Address | A18 to A2, 0, 1 | A18 to A2, 1, 0 | A18 to A2, 1, 1 | A18 to A2, 0, 0 |
| 2nd Burst Address | A18 to A2, 1, 0 | A18 to A2, 1, 1 | A18 to A2, 0, 0 | A18 to A2, 0, 1 |
| 3rd Burst Address | A18 to A2, 1, 1 | A18 to A2, 0, 0 | A18 to A2, 0, 1 | A18 to A2, 1, 0 |

**[μPD4481322, μPD4481362]**




**[μPD4481322, μPD4481362]**

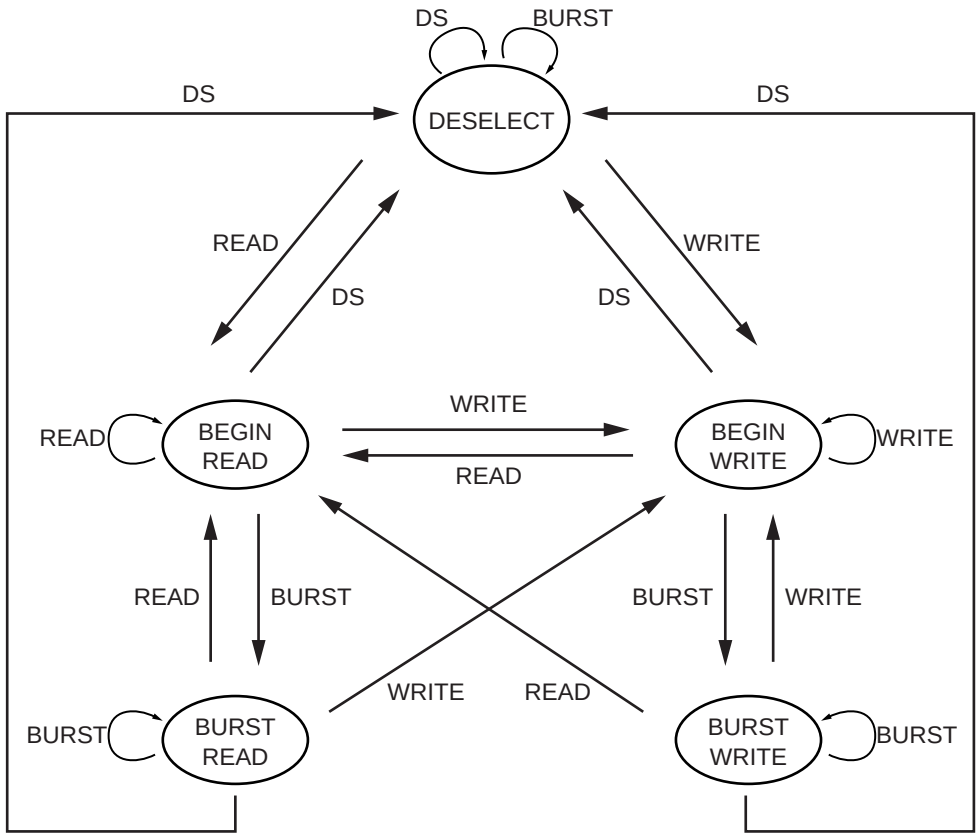
**Interleaved Burst Sequence Table (MODE = $V_{DD}$)**

| | |
|---|---|
| External Address | A17 to A2, A1, A0 |
| 1st Burst Address | A17 to A2, A1, /A0 |
| 2nd Burst Address | A17 to A2, /A1, A0 |
| 3rd Burst Address | A17 to A2, /A1, /A0 |

**Linear Burst Sequence Table (MODE = $V_{SS}$)**

| | | | | |
|---|---|---|---|---|
| External Address | A17 to A2, 0, 0 | A17 to A2, 0, 1 | A17 to A2, 1, 0 | A17 to A2, 1, 1 |
| 1st Burst Address | A17 to A2, 0, 1 | A17 to A2, 1, 0 | A17 to A2, 1, 1 | A17 to A2, 0, 0 |
| 2nd Burst Address | A17 to A2, 1, 0 | A17 to A2, 1, 1 | A17 to A2, 0, 0 | A17 to A2, 0, 1 |
| 3rd Burst Address | A17 to A2, 1, 1 | A17 to A2, 0, 0 | A17 to A2, 0, 1 | A17 to A2, 1, 0 |

**State Diagram**




| Command | Operation |
|---|---|
| DS | Deselect |
| Read | New Read |
| Write | New Write |
| Burst | Burst Read, Burst Write or Continue Deselect |

**Remarks 1.** States change on the rising edge of the clock.

**2.** A Stall or Ignore Clock Edge cycle is not shown in the above diagram. This is because /CKE HIGH only blocks the clock (CLK) input and does not change the state of the device.

**Asynchronous Truth Table**

| Operation | /G | I/O |
|---|---|---|
| Read Cycle | L | Dout |
| Read Cycle | H | High-Z |
| Write Cycle | × | High-Z, Din |
| Deselected | × | High-Z |

**Remark** × : don't care

**Synchronous Truth Table**

| Operation | /CE | CE2 | /CE2 | ADV | /WE | /BWs | /CKE | CLK | I/O | Address | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Deselected | H | × | × | L | × | × | L | L → H | High-Z | None | 1 |
| Deselected | × | L | × | L | × | × | L | L → H | High-Z | None | 1 |
| Deselected | × | × | H | L | × | × | L | L → H | High-Z | None | 1 |
| Continue Deselected | × | × | × | H | × | × | L | L → H | High-Z | None | 1 |
| Read Cycle / Begin Burst | L | H | L | L | H | × | L | L → H | Dout | External | |
| Read Cycle / Continue Burst | × | × | × | H | × | × | L | L → H | Dout | Next | |
| Write Cycle / Begin Burst | L | H | L | L | L | L | L | L → H | Din | External | |
| Write Cycle / Continue Burst | × | × | × | H | × | L | L | L → H | Din | Next | |
| Write Cycle / Write Abort | L | H | L | L | L | H | L | L → H | High-Z | External | |
| Write Cycle / Write Abort | × | × | × | H | × | H | L | L → H | High-Z | Next | |
| Stall / Ignore Clock Edge | × | × | × | × | × | × | H | L → H | – | Current | 2 |

**Notes 1.** Deselect status is held until new "Begin Burst" entry.

**2.** If an Ignore Clock Edge command occurs during a read operation, the I/O bus will remain active (low impedance). If it occurs during a write cycle, the bus will remain high impedance. No write operation will be performed during the Ignore Clock Edge cycle.

**Remarks 1.** × : don't care

**2.** /BWs = L means any one or more byte write enables (/BW1, /BW2, /BW3 or /BW4) are LOW.
/BWs = H means all byte write enables (/BW1, /BW2, /BW3 or /BW4) are HIGH.

**Partial Truth Table for Write Enables**

**[μPD4481162, μPD4481182]**

| Operation | /WE | /BW1 | /BW2 |
|---|---|---|---|
| Read Cycle | H | × | × |
| Write Cycle / Byte 1 (I/O [1:8], I/OP1) | L | L | H |
| Write Cycle / Byte 2 (I/O [9:16], I/OP2) | L | H | L |
| Write Cycle / All Bytes | L | L | L |
| Write Abort / NOP | L | H | H |

**Remark** × : don't care

**[μPD4481322, μPD4481362]**

| Operation | /WE | /BW1 | /BW2 | /BW3 | /BW4 |
|---|---|---|---|---|---|
| Read Cycle | H | × | × | × | × |
| Write Cycle / Byte 1 (I/O [1:8], I/OP1) | L | L | H | H | H |
| Write Cycle / Byte 2 (I/O [9:16], I/OP2) | L | H | L | H | H |
| Write Cycle / Byte 3 (I/O [17:24], I/OP3) | L | H | H | L | H |
| Write Cycle / Byte 4 (I/O [25:32], I/OP4) | L | H | H | H | L |
| Write Cycle / All Bytes | L | L | L | L | L |
| Write Abort / NOP | L | H | H | H | H |

**Remark** × : don't care

**ZZ (Sleep) Truth Table**

| ZZ | Chip Status |
|---|---|
| ≤ 0.2 V | Active |
| Open | Active |
| ≥ $V_{DD}$ – 0.2 V | Sleep |

## Electrical Specifications

### Absolute Maximum Ratings

| | Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| ★ | Supply voltage | $V_{DD}$ | | -A44, -A50, -A60, -A75<br>-A44Y, -A50Y, -A60Y, -A75Y | –0.5 | | +4.0 | V |
| | | | | -C60, -C75<br>-C60Y, -C75Y | –0.5 | | +3.0 | |
| | Output supply voltage | $V_{DDQ}$ | | | –0.5 | | $V_{DD}$ | V |
| | Input voltage | $V_{IN}$ | | | –0.5 Note | | $V_{DD}$ + 0.5 | V |
| | Input / Output voltage | $V_{I/O}$ | | | –0.5 Note | | $V_{DDQ}$ + 0.5 | V |
| ★ | Operating ambient temperature | $T_A$ | -A44, -A50, -A60, -A75, -C60, -C75 | | 0 | | 70 | °C |
| | | | -A44Y, -A50Y, -A60Y, -A75Y, -C60Y, -C75Y | | –40 | | +85 | |
| | Storage temperature | $T_{stg}$ | | | –55 | | +125 | °C |

**Note** –2.0 V (MIN.) (Pulse width : 2 ns)

**Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.**

### Recommended DC Operating Conditions (1/2)

| | Parameter | Symbol | Conditions | -A44, -A50, -A60, -A75<br>-A44Y, -A50Y, -A60Y, -A75Y | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | MIN. | TYP. | MAX. | |
| | Supply voltage | $V_{DD}$ | | 3.135 | 3.3 | 3.465 | V |
| | **2.5 V LVTTL Interface** | | | | | | |
| | Output supply voltage | $V_{DDQ}$ | | 2.375 | 2.5 | 2.9 | V |
| | High level input voltage | $V_{IH}$ | | 1.7 | | $V_{DDQ}$ + 0.3 | V |
| | Low level input voltage | $V_{IL}$ | | –0.3 Note | | +0.7 | V |
| | **3.3 V LVTTL Interface** | | | | | | |
| | Output supply voltage | $V_{DDQ}$ | | 3.135 | 3.3 | 3.465 | V |
| | High level input voltage | $V_{IH}$ | | 2.0 | | $V_{DDQ}$ + 0.3 | V |
| | Low level input voltage | $V_{IL}$ | | –0.3 Note | | +0.8 | V |

**Note** –0.8 V (MIN.) (Pulse width : 2 ns)

### Recommended DC Operating Conditions (2/2)

| | Parameter | Symbol | Conditions | -C60, -C75<br>-C60Y, -C75Y | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | MIN. | TYP. | MAX. | |
| | Supply voltage | $V_{DD}$ | | 2.375 | 2.5 | 2.625 | V |
| | Output supply voltage | $V_{DDQ}$ | | 2.375 | 2.5 | 2.625 | V |
| | High level input voltage | $V_{IH}$ | | 1.7 | | $V_{DDQ}$ + 0.3 | V |
| | Low level input voltage | $V_{IL}$ | | –0.3 Note | | +0.7 | V |

**Note** –0.8 V (MIN.) (Pulse width : 2 ns)

**DC Characteristics ($V_{DD}$ = 3.3 ± 0.165 V or 2.5 ± 0.125 V)**

| | Parameter | Symbol | Test condition | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| | Input leakage current | $I_{LI}$ | $V_{IN}$ (except ZZ, MODE) = 0 V to $V_{DD}$ | | –2 | | +2 | μA |
| | I/O leakage current | $I_{LO}$ | $V_{I/O}$ = 0 V to $V_{DD}$Q, Outputs are disabled. | | –2 | | +2 | μA |
| ★ | Operating supply current | $I_{DD}$ | Device selected, Cycle = MAX. $V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$, $I_{I/O}$ = 0 mA | -A44 -A44Y | | | 440 | mA |
| | | | | -A50 -A50Y | | | 400 | |
| | | | | -A60, -C60 -A60Y, -C60Y | | | 320 | |
| | | | | -A75, -C75 -A75Y, -C75Y | | | 300 | |
| | Standby supply current | $I_{SB}$ | Device deselected, Cycle = 0 MHz, $V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$, All inputs are static. | | | | 30 | mA |
| | | $I_{SB1}$ | Device deselected, Cycle = 0 MHz, $V_{IN} \leq$ 0.2 V or $V_{IN} \geq V_{DD}$ – 0.2 V, $V_{I/O} \leq$ 0.2 V, All inputs are static. | | | | 15 | |
| | | $I_{SB2}$ | Device deselected, Cycle = MAX. $V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$ | | | | 130 | |
| | Power down supply current | $I_{SBZZ}$ | ZZ ≥ $V_{DD}$ – 0.2 V, $V_{I/O} \leq V_{DD}$Q + 0.2 V | | | | 15 | mA |
| | **2.5 V LVTTL Interface** | | | | | | | |
| | High level output voltage | $V_{OH}$ | $I_{OH}$ = –2.0 mA | | 1.7 | | | V |
| | | | $I_{OH}$ = –1.0 mA | | 2.1 | | | |
| | Low level output voltage | $V_{OL}$ | $I_{OL}$ = +2.0 mA | | | | 0.7 | V |
| | | | $I_{OL}$ = +1.0 mA | | | | 0.4 | |
| | **3.3 V LVTTL Interface** | | | | | | | |
| | High level output voltage | $V_{OH}$ | $I_{OH}$ = –4.0 mA | | 2.4 | | | V |
| | Low level output voltage | $V_{OL}$ | $I_{OL}$ = +8.0 mA | | | | 0.4 | V |

**Capacitance ($T_A$ = 25 °C, f = 1MHz)**

| Parameter | Symbol | Test condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | $V_{IN}$ = 0 V | | | 6.0 | pF |
| Input / Output capacitance | $C_{I/O}$ | $V_{I/O}$ = 0 V | | | 8.0 | pF |
| Clock input capacitance | $C_{clk}$ | $V_{clk}$ = 0 V | | | 6.0 | pF |

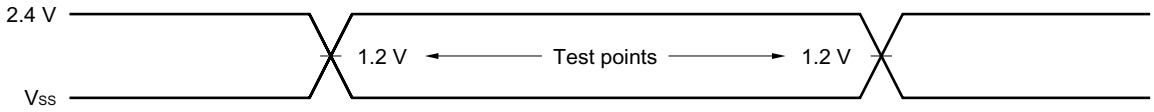
**Remark** These parameters are periodically sampled and not 100% tested.

**AC Characteristics ($V_{DD}$ = 3.3 ± 0.165 V or 2.5 ± 0.125 V)**

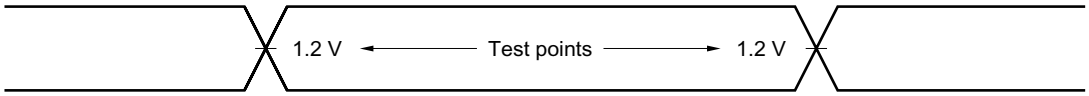
**AC Test Conditions**

**2.5 V LVTTL Interface**

**Input waveform (Rise / Fall time ≤ 2.4 ns)**

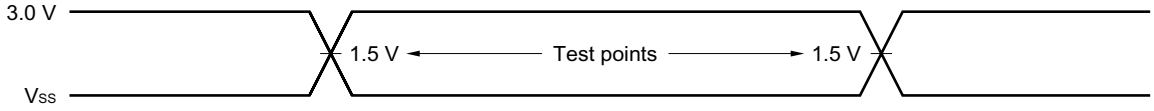



**Output waveform**

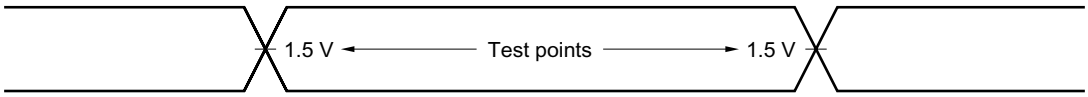



**3.3 V LVTTL Interface**

**Input waveform (Rise / Fall time ≤ 3.0 ns)**




**Output waveform**

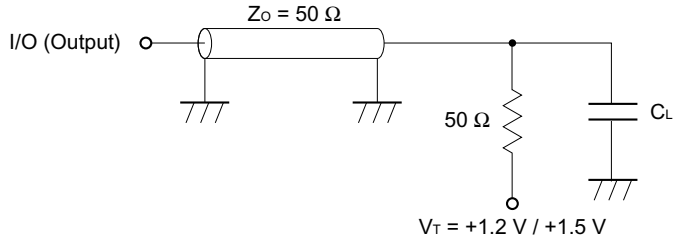



**Output load condition**

$C_L$ : 30 pF

5 pF (TKHQX1, TKHQX2, TGLQX, TGHQZ, TKHQZ)

**Figure External load at test**




**Remark** $C_L$ includes capacitances of the probe and jig, and stray capacitances.

**Read and Write Cycle (2.5 V LVTTL Interface)**

★

| Parameter | | Symbol | | -A44, -A50, -A60, -C60<br>-A44Y, -A50Y, -A60Y, -C60Y<br>(167 MHz) | | -A75, -C75<br>-A75Y, -C75Y<br>(133 MHz) | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Standard | Alias | MIN. | MAX. | MIN. | MAX. | | |
| Cycle time | | TKHKH | TCYC | 6 | – | 7.5 | – | ns | |
| Clock access time | | TKHQV | TCD | – | 3.5 | – | 4.2 | ns | |
| Output enable access time | | TGLQV | TOE | – | 3.5 | – | 4.2 | ns | |
| Clock high to output active | | TKHQX1 | TDC1 | 1.5 | – | 1.5 | – | ns | 1, 2 |
| Clock high to output change | | TKHQX2 | TDC2 | 1.5 | – | 1.5 | – | ns | |
| Output enable to output active | | TGLQX | TOLZ | 0 | – | 0 | – | ns | 1 |
| Output disable to output High-Z | | TGHQZ | TOHZ | 0 | 3.5 | 0 | 4.2 | ns | 1 |
| Clock high to output High-Z | | TKHQZ | TCZ | 1.5 | 3.5 | 1.5 | 3.5 | ns | 1, 2 |
| Clock high pulse width | | TKHKL | TCH | 1.8 | – | 2.2 | – | ns | |
| Clock low pulse width | | TKLKH | TCL | 1.8 | – | 2.2 | – | ns | |
| Setup times | Address | TAVKH | TAS | 1.5 | – | 1.5 | – | ns | |
| | Address advance | TADVVKH | TADVS | | | | | | |
| | Clock enable | TEVKH | TCES | | | | | | |
| | Chip enable | TCVKH | TCSS | | | | | | |
| | Data in | TDVKH | TDS | | | | | | |
| | Write enable | TWVKH | TWS | | | | | | |
| Hold times | Address | TKHAX | TAH | 0.5 | – | 0.5 | – | ns | |
| | Address advance | TKHADVX | TADVH | | | | | | |
| | Clock enable | TKHEX | TCEH | | | | | | |
| | Chip enable | TKHCX | TCSH | | | | | | |
| | Data in | TKHDX | TDH | | | | | | |
| | Write enable | TKHWX | TWH | | | | | | |
| Power down entry time | | TZZE | TZZE | – | 12 | – | 15 | ns | |
| Power down recovery time | | TZZR | TZZR | – | 12 | – | 15 | ns | |

**Notes 1.** Transition is measured ±200 mV from steady state.

**2.** To avoid bus contention, the output buffers are designed such that TKHQZ (device turn-off) is faster than TKHQX1 (device turn-on) at a given temperature and voltage. The specs as shown do not imply bus contention because TKHQX1 is a min. parameter that is worse case at totally different conditions ($T_A$ min., $V_{DD}$ max.) than TKHQZ, which is a max. parameter (worse case at $T_A$ max., $V_{DD}$ min.).

**Read and Write Cycle (3.3 V LVTTL Interface)**

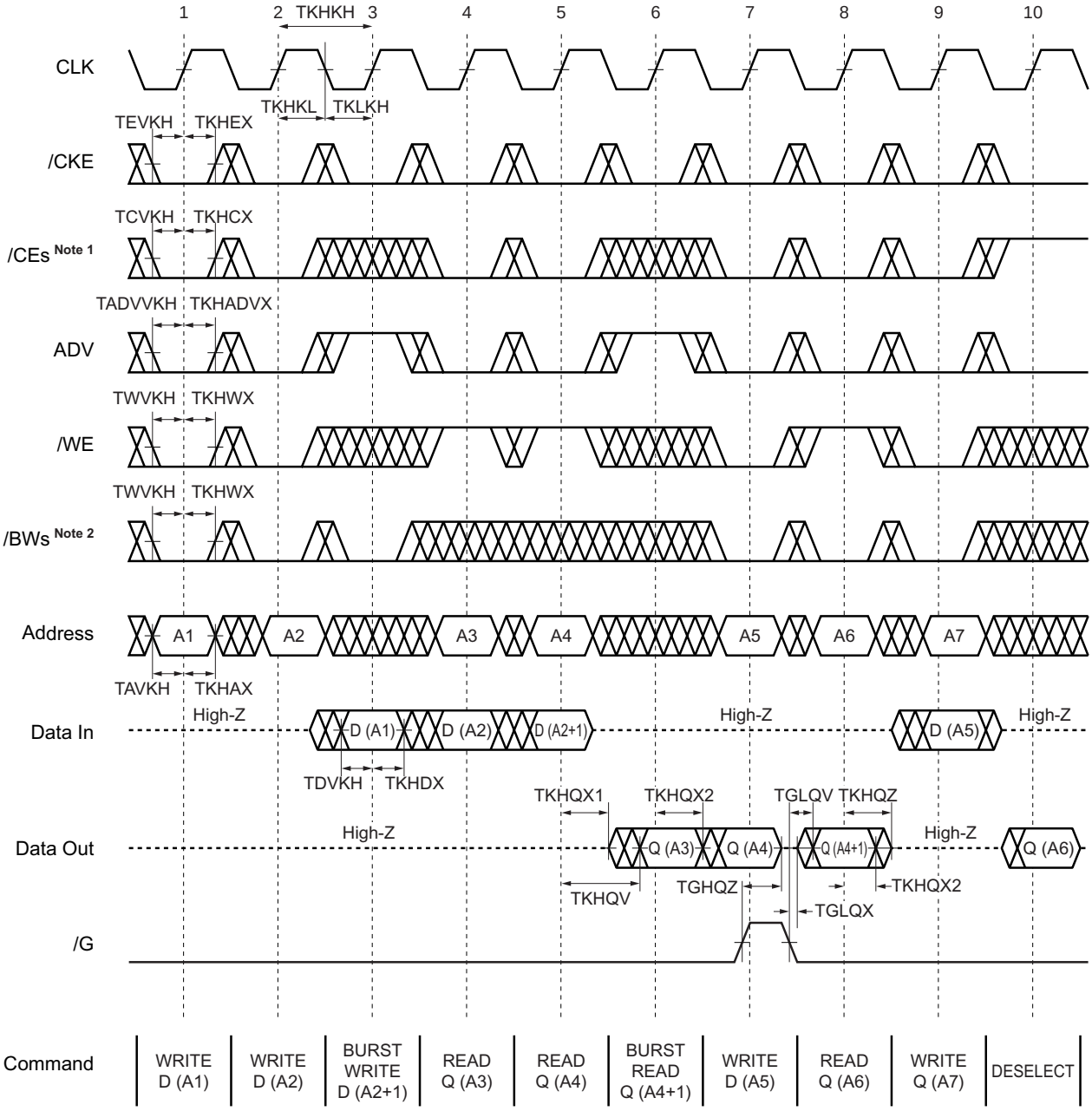
★

| Parameter | | Symbol | | -A44 -A44Y (225 MHz) | | -A50 -A50Y (200 MHz) | | -A60 -A60Y (167 MHz) | | -A75 -A75Y (133 MHz) | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Standard | Alias | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| Cycle time | | TKHKH | TCYC | 4.4 | – | 5 | – | 6 | – | 7.5 | – | ns | |
| Clock access time | | TKHQV | TCD | – | 2.8 | – | 3.2 | – | 3.5 | – | 4.2 | ns | |
| Output enable access time | | TGLQV | TOE | – | 2.8 | – | 3.2 | – | 3.5 | – | 4.2 | ns | |
| Clock high to output active | | TKHQX1 | TDC1 | 1.5 | – | 1.5 | – | 1.5 | – | 1.5 | – | ns | 1, 2 |
| Clock high to output change | | TKHQX2 | TDC2 | 1.5 | – | 1.5 | – | 1.5 | – | 1.5 | – | ns | |
| Output enable to output active | | TGLQX | TOLZ | 0 | – | 0 | – | 0 | – | 0 | – | ns | 1 |
| Output disable to output High-Z | | TGHQZ | TOHZ | 0 | 2.8 | 0 | 3.2 | 0 | 3.5 | 0 | 4.2 | ns | 1 |
| Clock high to output High-Z | | TKHQZ | TCZ | 1.5 | 2.8 | 1.5 | 3.2 | 1.5 | 3.5 | 1.5 | 3.5 | ns | 1, 2 |
| Clock high pulse width | | TKHKL | TCH | 1.8 | – | 1.8 | – | 1.8 | – | 2.2 | – | ns | |
| Clock low pulse width | | TKLKH | TCL | 1.8 | – | 1.8 | – | 1.8 | – | 2.2 | – | ns | |
| Setup times | Address | TAVKH | TAS | 1.4 | – | 1.5 | – | 1.5 | – | 1.5 | – | ns | |
| | Address advance | TADVVKH | TADVS | | | | | | | | | | |
| | Clock enable | TEVKH | TCES | | | | | | | | | | |
| | Chip enable | TCVKH | TCSS | | | | | | | | | | |
| | Data in | TDVKH | TDS | | | | | | | | | | |
| | Write enable | TWVKH | TWS | | | | | | | | | | |
| Hold times | Address | TKHAX | TAH | 0.4 | – | 0.5 | – | 0.5 | – | 0.5 | – | ns | |
| | Address advance | TKHADVX | TADVH | | | | | | | | | | |
| | Clock enable | TKHEX | TCEH | | | | | | | | | | |
| | Chip enable | TKHCX | TCSH | | | | | | | | | | |
| | Data in | TKHDX | TDH | | | | | | | | | | |
| | Write enable | TKHWX | TWH | | | | | | | | | | |
| Power down entry time | | TZZE | TZZE | – | 8.8 | – | 10 | – | 12 | – | 15 | ns | |
| Power down recovery time | | TZZR | TZZR | – | 8.8 | – | 10 | – | 12 | – | 15 | ns | |

**Notes 1.** Transition is measured ±200 mV from steady state.

**2.** To avoid bus contention, the output buffers are designed such that TKHQZ (device turn-off) is faster than TKHQX1 (device turn-on) at a given temperature and voltage. The specs as shown do not imply bus contention because TKHQX1 is a min. parameter that is worse case at totally different conditions ($T_A$ min., $V_{DD}$ max.) than TKHQZ, which is a max. parameter (worse case at $T_A$ max., $V_{DD}$ min.).

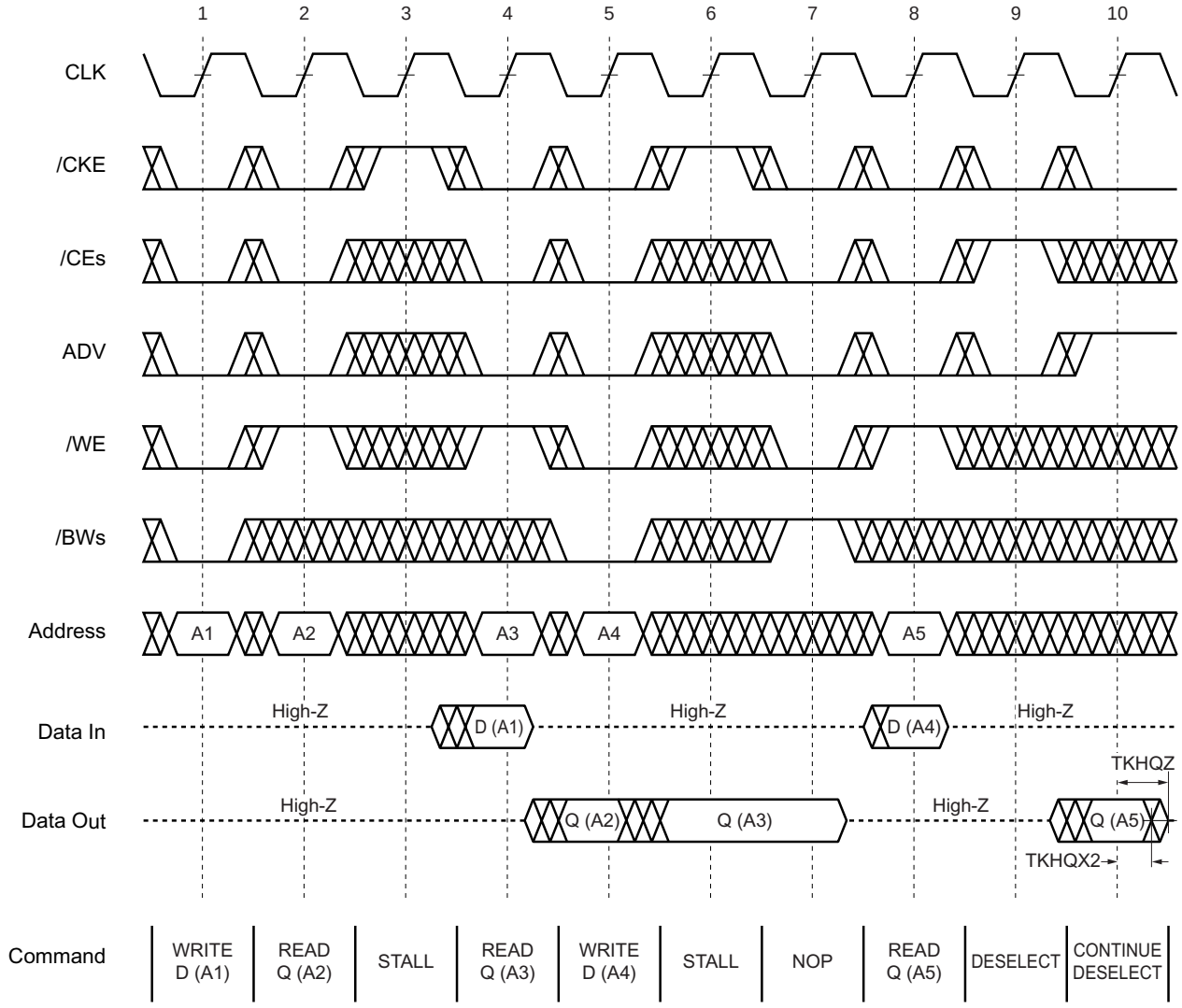
**READ / WRITE CYCLE**



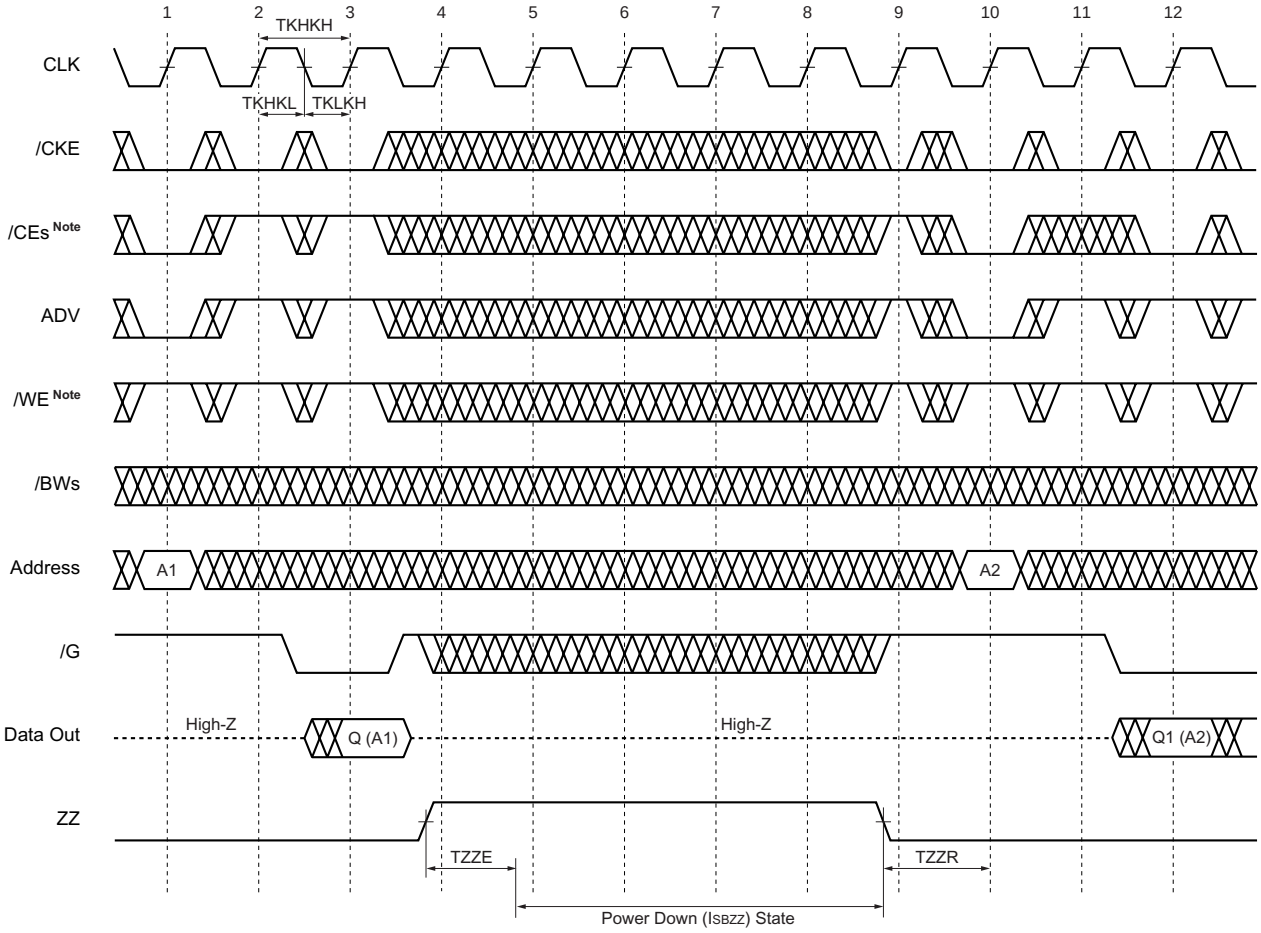

**Notes 1.** /CEs refers to /CE, CE2 and /CE2. When /CEs is LOW, /CE and /CE2 are LOW and CE2 is HIGH. When /CEs is HIGH, /CE and /CE2 are HIGH and CE2 is LOW.

**2.** /BWs refers to /BW1, /BW2, /BW3 and /BW4. When /BWs is LOW, any one or more byte write enables (/BW1, /BW2, /BW3 or /BW4) are LOW.

**NOP, STALL AND DESELECT CYCLE**



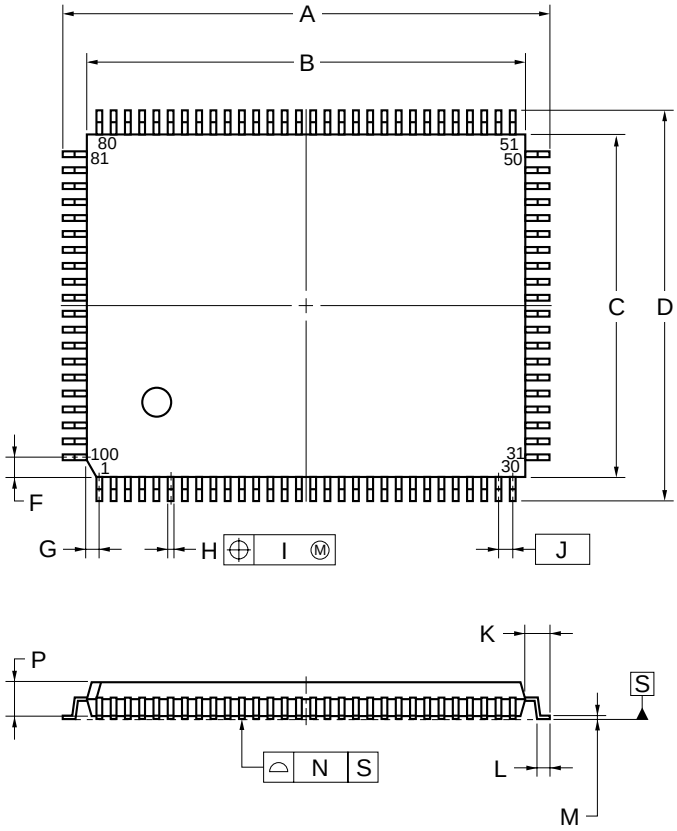
**POWER DOWN (ZZ) CYCLE**

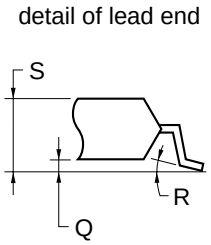



**Note** /WE or /CEs must be held HIGH at CLK rising edge (clock edge No.2 and No.3 in this figure) prior to power down state entry.

**Package Drawing**

## 100-PIN PLASTIC LQFP (14x20)




**NOTE**

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS |
|---|---|
| A | 22.0±0.2 |
| B | 20.0±0.2 |
| C | 14.0±0.2 |
| D | 16.0±0.2 |
| F | 0.825 |
| G | 0.575 |
| H | $0.32^{+0.08}_{-0.07}$ |
| I | 0.13 |
| J | 0.65 (T.P.) |
| K | 1.0±0.2 |
| L | 0.5±0.2 |
| M | $0.17^{+0.06}_{-0.05}$ |
| N | 0.10 |
| P | 1.4 |
| Q | 0.125±0.075 |
| R | $3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$ |
| S | 1.7 MAX. |

**S100GF-65-8ET-1**

**Recommended Soldering Condition**

Please consult with our sales offices for soldering conditions of the μPD4481162, 4481182, 4481322 and 4481362.

**Types of Surface Mount Devices**

| | |
|---|---|
| μPD4481162GF | : 100-pin PLASTIC LQFP (14 x 20) |
| μPD4481182GF | : 100-pin PLASTIC LQFP (14 x 20) |
| μPD4481322GF | : 100-pin PLASTIC LQFP (14 x 20) |
| μPD4481362GF | : 100-pin PLASTIC LQFP (14 x 20) |

**Revision History**

| Edition/ Date | Page | | Type of revision | Location | Description (Previous edition → This edition) |
|---|---|---|---|---|---|
| | This edition | Previous edition | | | |
| 3rd edition/ Dec. 2002 | Throughout | Throughout | Modification<br>Addition | –<br>– | Preliminary Data Sheet → Data Sheet<br>Extended operating temperature products ($T_A$ = –40 to +85 °C) |

**[MEMO]**

**[MEMO]**

**[MEMO]**

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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